In the specification:

Please substitute the following paragraphs for the paragraphs at the indicated locations in the specification as originally filed or most recently amended.

Page 3, line 5+:

Dynamic threshold voltage MOSFETs (DTMOSFETs) are known and an exemplary design is disclosed in U. S. Patent ~~5,539,368~~ 5,559,368. A schematic depiction of this transistor is illustrated in Figure 1. This transistor design seeks to maintain high performance at reduced power supply voltage by connecting the gate of the transistor to the silicon well in which the transistor is formed and can achieve a high drive current in the "on" state as well as low "off" state leakage current. In the "off" state, Vgs = Vbs = 0V and the transistor has a high threshold. In the "on" state, Vgs = Vds = Vbs and has a low threshold because gate voltage is applied to the body of the transistor. However, the principal disadvantage of this transistor design is that because gate bias is applied to the transistor body, the leakage current of the forward biased p-n junction at the source increases dramatically when the power supply voltage is greater than 0.7V; effectively limiting the power supply voltage to that value; a value which increases noise susceptibility and does not support sufficient voltage overdrive for optimal or potential switching speed.

Page 6, line 22+:

The transistor in accordance with the invention is preferably formed on a silicon-on-insulator substrate comprising a thick handling substrate 12, an insulator 14 (generally oxide and referred to as a buried oxide (BOX) layer) and a relatively thin, high-quality monocrystalline semiconductor layer (in this case of p-

type), generally silicon. However, it should be understood that the basic principles of the invention are also applicable to other semiconductor or substrate structures, such as SiGe or GaAs. As illustrated, the field effect transistor portion 10', itself, of the DTMOSFET is positioned at the left side of Figure 2 and Figure 3 and in Figure 3 the source and drain regions (S/D)are positioned one in front of (or behind) the other with the conduction channel extending in a direction perpendicular to the plane of the page.

Page 8, line 17+:

Therefore, the DTMOSFET in accordance with the invention has the following advantages:

1.) The transistor can have a high threshold in the off-state and a low threshold in the on-state to produce a high Ion and low Ioff and improved on/off current ratio.

2.) The power supply voltage can be scaled down due to the low threshold in the on-state and power consumption/dissipation can be reduced.

3.) There is no floating body effect in the transistor even though "gate" 20 disconnects the transistor portion channel from the p-well contact. (In the on-state the transistor has a floating p-well and the body can rise to the same potential as the source voltage. For the partially depleted SOI MOSFET, the floating body potential depends on how recently the and how often the transistor has been switched through its high impact ionization condition. However, with the transistor structure in accordance with the invention, the p-well is connected to the p-well contact 18 in the off-state and the charge stored in the p-well is easily removed.)

4. Unlike the prior DTMOSFET of Figure 1, the gate of transistor portion is not directly connected to the p-well contact and there is no forward p-n junction

leakage or criticality of power supply voltage that can cause increased leakage.